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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,780	03/23/2004	Susumu Okazaki	1111.70127	2380

7590 03/30/2007

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EXAMINER	
A, MINH D	
ART UNIT	PAPER NUMBER
2821	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,780	OKAZAKI ET AL.	
	Examiner	Art Unit	
	Minh D. A	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 6, 8-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Park et al (Patent No; 6, 870, 186).

Regarding claim 1, figures 1 and 5, Park discloses that, an organic electroluminescent display device comprising a first substrate (130) having of light emitting elements on one surface and a second substrate (110) having thereon a circuit (TFT)(120) for controlling the plurality of the light emitting elements (E), the second substrate (110) being bonded to the one surface of the first substrate (130) and a sealing pattern (140) for sealing a space where the plurality of the light emitting elements (E) are formed. Col.7, 45-67 to col.9, lines 1-56.

Regarding claim 2, figures 1 and 5, Park discloses that, the display device includes: a plurality of scan bus lines (scanning lines); a plurality of data bus lines intersecting the plurality of the scan bus lines; and a plurality of switching elements (E) arranged respectively at intersections between the plurality of scan bus lines and the

plurality of data bus lines and electrically connected to the respective plurality of the light emitting elements. Col.2, lines 33-63.

Regarding claim 3, figures 1 and 5, Park discloses that, a first substrate (130) having a plurality of light emitting elements (E) on one surface thereof; and a second substrate (110) having thereon a circuit (TFT) for controlling the plurality of the light emitting elements (E), the second substrate (110) being bonded to the one surface of the first substrate (130), and a seal pattern (140) for sealing a space where the plurality of the light emitting elements (E) are formed, wherein a plurality of scan (scan) bus lines, a plurality of data (data) bus lines intersecting the plurality of scan bus lines, and a plurality of switching elements(E) arranged respectively at intersections between the plurality of scan bus lines and the plurality of data bus lines and electrically connected to the respective plurality of the light emitting elements are formed on the first substrate. Col.2, lines 33-63 and col.7, 45-67 to col.9, lines 1-56.

Regarding claim 6, Park discloses the second substrate being a printed circuit board. See figures 1 and 5.

Regarding claim 8, Park discloses that, the light emitting elements (E) are organic EL elements. See figures 1 and 5.

Regarding claim 9, figures 1 and 5, Park discloses that, the first substrate (130) and the second substrate (110) are electrically connected to each other by columnar electrodes formed between the first substrate and the second substrate.

Regarding claims 10 and 11, figures 1 and 5, Park discloses that, the first substrate and the second substrate are electrically connected to each other by a flexible substrate.

Regarding claim 12, figure 5, Park discloses that, (E) for forming a plurality of light emitting elements on one surface of a first substrate (130); a TFT (120) for forming a plurality of switching elements on one surface of a second substrate (110); bonding the one surface of the first substrate and said one surface of the second substrate to each other and electrically connecting said respective plurality of the light emitting elements to the respective plurality of switching elements.

Regarding claim 13, figures 1 and 5, Park discloses a substrate (130) for forming on one surface of a first substrate a plurality of light emitting elements (E) and a plurality of switching elements (TFT) electrically connected to said respective plurality of light emitting elements (E); a substrate (110) for forming on one surface of a second substrate a prescribed circuit which is to be electrically connected to said plurality of switching elements (TFT); and a seal pattern (140) for bonding the first substrate (130) and the second substrate(110) to each other with the one surface of the first substrate and the one surface of the second substrate opposed to each other to electrically connect the circuit to the plurality of switching elements (TFT). Col.7, 45-67 to col.9, lines 1-56.

Regarding claim 14, Park discloses a seal pattern (140) for bonding the first substrate (130) and the second substrate (110) to each other, the first substrate (130) and the second substrate (110) are bonded to each other via a sealing_compound, to

seal a space where said plurality of light emitting elements are formed and a gas is sealed within said space. Col.7, 45-67 to col.9, lines 1-56.

Regarding claim 15, figures 1 and 5, Park discloses a seal pattern (140) for bonding the first substrate and the second substrate to each other, the first substrate and the second substrate are bonded to each other, via a sealing; compound to seal a space where said plurality of light emitting elements are formed wherein a gas is sealed within said space.

Regarding claims 16-17, figures 1 and 5, Park discloses that, the light emitting elements (E) are organic EL elements and the first substrate and the second substrate are electrically connected to each other by columnar electrodes formed between the first substrate and the second substrate.

Regarding claims 18-20, figures 1 and 5, Park discloses that, the first substrate and the second substrate are electrically connected to each other by a flexible substrate and a light emitted by the light emitting elements is taken out toward the other surface of the first substrate and a sealing compound for sealing a gas within said space defined between said first substrate and said second substrate. Col.2, lines 33-63 and col.7, 45-67 to col.9, lines 1-56.

Regarding claims 21-22, figures 1 and 5, Park discloses that, a sealing compound for sealing a gas within said space defined between said first substrate and said second substrate and the light emitting element and the switching element are positioned so as to overlap in a normal direction of the first substrate and the second substrate. Col. 2, lines 33-63 and col.7, 45-67 to col.9, lines 1-56.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Park et al (Patent No; 6, 870, 186) in view of Akimoto et al (Patent No: US 6, 950, 081).

Regarding claims 4-5, Park discloses that, the display device having a scan lines and data lines.

However, Park does not teach that, a scan bus line control circuit for controlling signals inputted into the plurality of scan bus lines, and a data bus line control circuit for controlling signals outputted from the plurality of data bus lines are formed on the first substrate.

Akimoto discloses that, an image display device includes a scan bus line control circuit (22) for controlling signals inputted into the plurality of scan bus lines, and a data bus line control circuit (21) for controlling signals outputted from the plurality of data bus lines. Col.4, lines 40-67 to col.7, lines 1-57.

It would have been an obvious to one of ordinary skill in the art at the time the invention was made to employ the scan bus line control circuit (22) for controlling signals inputted into the plurality of scan bus lines, and a data bus line control circuit (21) for controlling signals outputted from the plurality of data bus lines such as that

suggested by Akimoto in the display device of Park to improve a display quality and improve to attain a gradation display by controlling the emission intensity of the light emittings.

Regarding claim 7, Park as modified, discloses the second substrate being a printed circuit board. See figures 1 and 5.

Citation of relevant prior art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Isami et al (US 6,791,521) and Yamazaki et al. (US 6,563,482) are cited to show a display device.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Dieu A whose telephone number is (571) 272-1817. The examiner can normally be reached on M-F (5:30 AM-2: 45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Owens Douglas W can be reached on (571) 272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner

Minh A

Art Unit 2821

3/24/07

SHIH-CHAO CHEN
PRIMARY EXAMINER